

[illegible]

- Active
  - L1: (8) ("6,529,410") or ("6,295,227") or ("5,640,032") or ("5,070,032") or ("5,9
  - L2: (2) ("20020093073") or ("20040070021")):PN.
  - L3: (30778) floating.clm.
  - L4: (3117) 3 and (sidewall\$1 or (side adj wall\$1)).clm.
  - L5: (1324) 4 and (floating adj gate).clm.
  - L6: (531) 5 and (opening\$1.clm. or trench\$2.clm.)
  - L7: (411) 6 and dielectric
  - L8: (409) 7 and etch\$3
  - L9: (360) 8 and (first near10 (float\$3 or gate\$5))
  - L10: (360) 9 and (first near "10" floating)
  - L11: (319) 9 and (first near10 floating)
  - L12: (318) 11 and (array or memory or (non adj volatile))
  - L13: (250) 12 and (first near10 floating).clm.
  - L14: (211) 13 and (second near10 floating)
  - L15: (164) 14 and (second near10 floating).clm.
- Failed
- Saved
  - (0) ("(thinadjfilm)nearresistor"):PN.
  - (0) ("(thinadjfilm)nearresistor"):PN.

	U	I	PT	P	Document ID	Issue Date	Pages	Title	Current OR	Current XB	Retrieval	Inventor	S	C	3	4	5
174	P	C	C	P	US 5429970	19950704		Method of making flash EEPROM memory cell	438/259	257/316, 257/E21.68		Hong, Gary	C	C	C	C	C
175	P	C	C	P	US 5413946	19950509		Method of making flash memory cell with self-aligning vertical channel	438/261	257/316, 257/E21.42		Hong, Gary	C	C	C	C	C
176	P	C	C	P	US 5380672	19950110		Dense vertical programmable read-only memory	438/257	257/E27.10		Yuan, Jack H. et al.	C	C	C	C	C
177	P	C	C	P	US 5315142	19940524		High performance trench EEPROM cell	257/316	257/321, 257/513		Acovic, Alexandre et al.	C	C	C	C	C
178	P	C	C	P	US 5238855	19930824		Cross-point contact-free array with non-volatile memory	438/261	257/E27.10		Gill, Manzur	C	C	C	C	C
179	P	C	C	P	US 5225361	19930706		Semiconductor memory device	438/264	257/E21.42		Kakiuchi, Takao et al.	C	C	C	C	C
180	P	C	C	P	US 5135879	19920804		Method of fabricating a high density EPROM cell	438/259	148/DIG.16		Richardson, William F.	C	C	C	C	C
181	P	C	C	P	US 5087584	19920211		Process for fabricating a contactless floating gate EPROM cell	438/262	148/DIG.50		Wada, Glen N. et al.	C	C	C	C	C
182	P	C	C	P	US 5087583	19920211		Process for EEPROM cell structure and architecture	438/260	257/E29.30		Hazani, Emanuel	C	C	C	C	C
183	P	C	C	P	US 5017977	19910521		Dual EPROM cells on trench walls with vertical channel	257/316	257/331, 257/E27.10		Richardson, William F.	C	C	C	C	C
184	P	C	C	P	US 4990979	19910205		Non-volatile memory cell	257/321	257/316, 257/397		Otto, Joachim	C	C	C	C	C